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ABSTRACT

A bidirectional digital data communication system which generate phase coherent upstream clock and carrier signals from recovered downstream clock generated from a master clock in a central unit. The preferred species uses any downstream clock rate and generates a phase coherent upstream clock so long as the two clock rates can be related by the ratio M/N where M and N are integers. One embodiment uses an MCNS downstream and an SCDMA upstream and uses MNCN timestamp messages in the downstream to achieve an estimate of RU frame offset prior to establishing frame alignment using a ranging process. The use of timestamp messages to estimate the offset is aided by a low jitter method for inserting timestamp messages by avoiding straddling of MPEG packet headers with the sync message. Clock slip is detected by counting upstream clock cycles over a predetermined downstream clock interval and the RU transmitter is shut down if slip is detected to prevent ISI interference from misaligned codes. An SCDMA transmitter for the minislot environment of 802.14 and MCNS is disclosed along with a receiver for the minislot environment using TDMA or SCDMA demultiplexing.